

Design Space Exploration for Complex Automotive Applications: An Engine Control System Case Study

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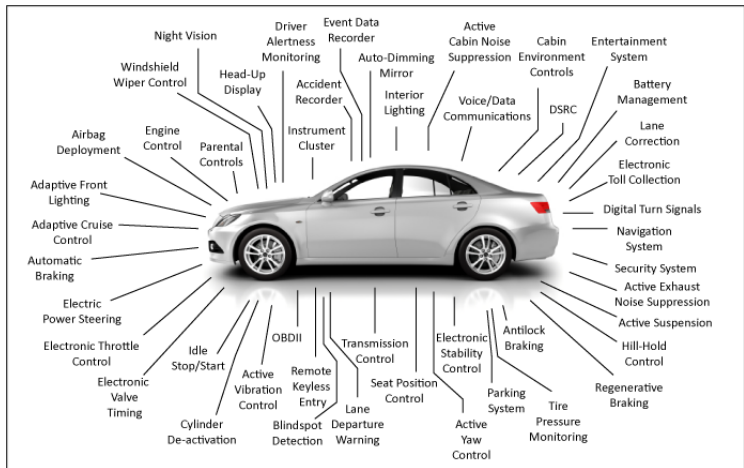
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UNIVERSITY *of* York



Motivations



Source: <http://www.chipsetc.com>

This Work

Objectives

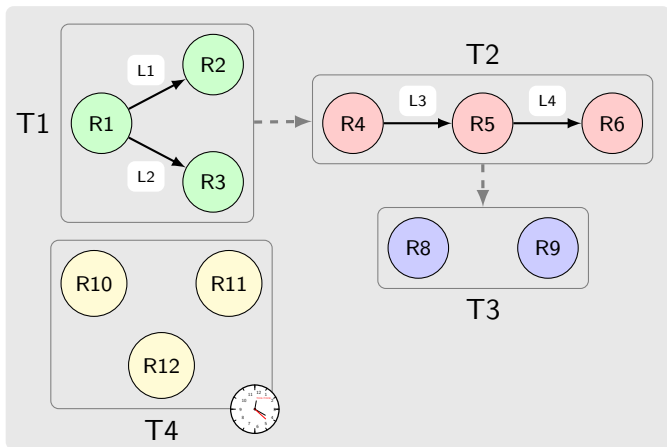
- ▶ Simulation framework
 - ▶ Rapid prototyping
 - ▶ Easily configurable
- ▶ Design space exploration of an automotive application

Hypotheses

- ▶ Application described using AMALTHEA¹
- ▶ Distributed memory multi-core platform

¹<http://www.amalthea-project.org>

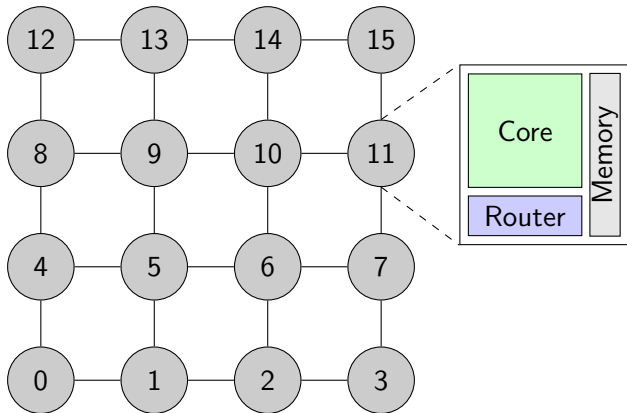
AMALTHEA



Application



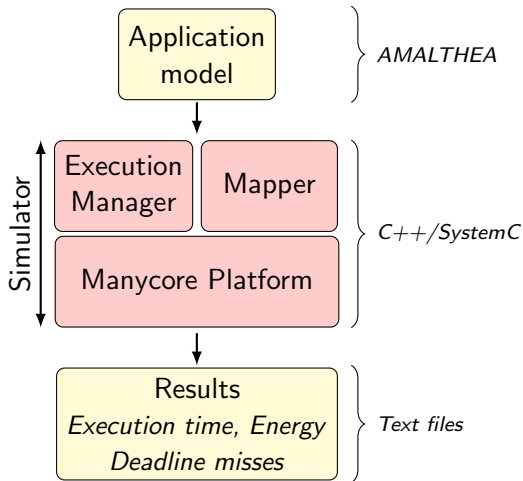
Simulated Hardware



Priority-Preemptive Arbitration NoC²

²Evgeny Bolotin et al. "QNoC: QoS architecture and design process for network on chip". In: *JOURNAL OF SYSTEMS ARCHITECTURE* 50 (2004), pp. 105–128.

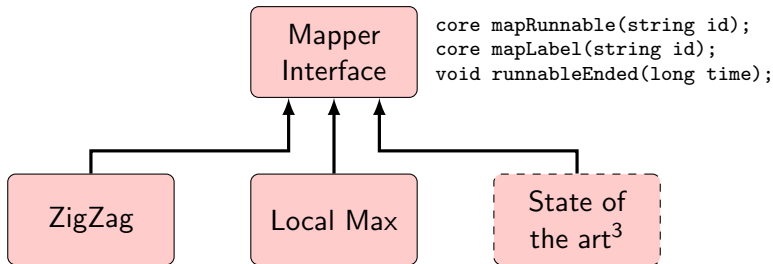
Simulation Framework Overview



Mapper

Responsibilities

- ▶ Map runnables on cores
- ▶ Map labels on memories



³A.K. Singh et al. "Mapping on multi/many-core systems: Survey of current and emerging trends". In: *50th ACM / EDAC / IEEE Design Automation Conference (DAC)*. 2013.

Cores Simulator

Speed vs Accuracy dilemma

- ▶ Based on information from AMALTHEA
- ▶ Transaction Level Modeling with Time (TLM-T)

Cores Simulator

Speed vs Accuracy dilemma

- ▶ Based on information from AMALTHEA
- ▶ Transaction Level Modeling with Time (TLM-T)

Configurable

- ▶ Different schedulers
- ▶ Different type of cores
 - ▶ Clock frequency
 - ▶ Energy efficiency

NoC Simulator

Speed vs Accuracy dilemma

- ▶ Transaction Level Modeling with Time (TLM-T)
- ▶ Only simulate packets entering/leaving the NoC⁴

⁴Leandro Soares Indrusiak, James Harbin, and Osmar Marchi dos Santos. "Fast Simulation of Networks-on-Chip with Priority-Preemptive Arbitration". In: *ACM Transactions on Design Automation of Electronic Systems* 20.4 (Sept. 2015), p. 22.

NoC Simulator

Speed vs Accuracy dilemma

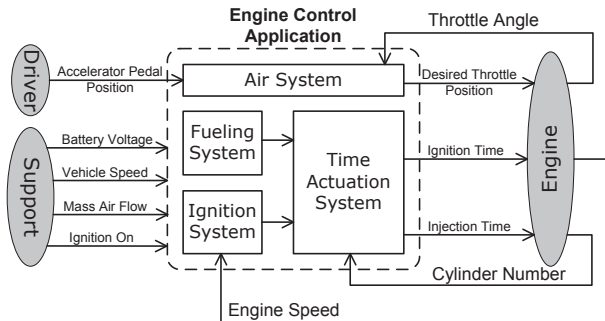
- ▶ Transaction Level Modeling with Time (TLM-T)
- ▶ Only simulate packets entering/leaving the NoC⁴

Configurable

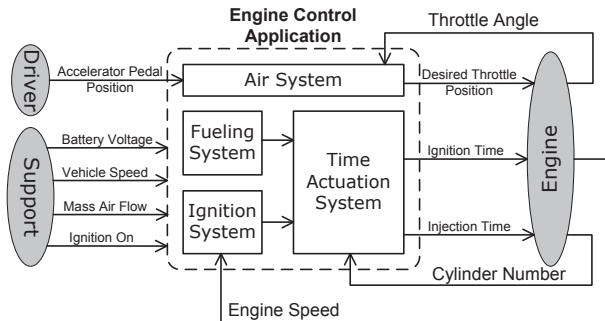
- ▶ NoC size
- ▶ Hop latency
- ▶ Router latency
- ▶ Full duplex or not ?

⁴Leandro Soares Indrusiak, James Harbin, and Osmar Marchi dos Santos. "Fast Simulation of Networks-on-Chip with Priority-Preemptive Arbitration". In: *ACM Transactions on Design Automation of Electronic Systems* 20.4 (Sept. 2015), p. 22.

Engine Control System Case Study



Engine Control System Case Study



AMALTHEA model

- ▶ 109 tasks
- ▶ 1239 runnables
- ▶ 10436 labels

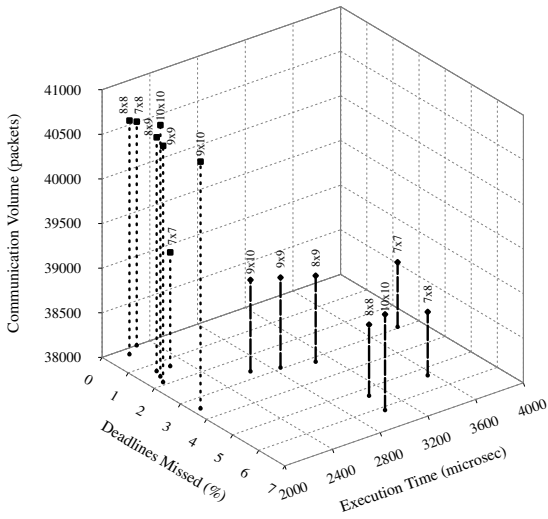
Exploration

Parameters

- ▶ NoC size
- ▶ Mapper
- ▶ Scheduler, Frequency, ...

NoC Size	Simulation Time (sec.)		Execution Time (μ s)		Deadline misses (%)		#Packets in NoC		APL (ns)	
	Loc.	ZZ	Loc.	ZZ	Loc.	ZZ	Loc.	ZZ	Loc.	ZZ
7 \times 7	30	24	3833	2282	2.9	1.3	38724	39275	108	115
7 \times 8	33	26	3560	2290	5.3	Ref	38711	40507	108	121
8 \times 8	32	27	3069	2172	5.3	0.2	38797	40619	116	120
8 \times 9	35	32	3090	2166	3.2	1.3	38964	40620	116	136
9 \times 9	36	33	2852	2102	2.9	1.8	39009	40648	119	134
9 \times 10	39	37	2659	2065	2.6	3.4	39025	40766	119	141
10 \times 10	48	44	3026	2138	6.1	1.6	39073	40817	116	147

Execution time vs Deadline missed vs Comm. volume



Conclusion

- ▶ Fully operational simulation flow
- ▶ To be released soon⁵

Perspectives

- ▶ Other input formats
- ▶ Different accuracy levels
- ▶ Analyses of the results

⁵<https://github.com/DreamCloud-Project>